ANNEXURE 2

Request for Proposal for Transfer of Technology for Gallium Arsenide based RF and Photonics Devices

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Contents

1 Introduction

Semi-Conductor Laboratory (SCL), an autonomous body under Department of Space, Government of India, is engaged in Research & Development in the area of Microelectronics. SCL has integrated facilities / supporting infrastructure and undertakes activities focused on design, development, fabrication, assembly and packaging, testing and quality assurance of CMOS and MEMS devices for various applications. SCL has 8" wafer fabrication line with 0.18µm CMOS process technology and a 6" wafer fabrication line with CMOS / MEMS process capability. Commensurate with the requirements of the fab lines, support infrastructure, namely clean rooms, high purity systems, utility plants and distribution network are operational on 24×7 basis.

SCL is looking for competent manufacturers / developers having sufficient technical expertise in design and development of monolithically integrated RF and photonics devices based on Gallium Arsenide technology including Vertical Cavity Surface Emitting Lasers (VCSELs), Photodetectors and Photovoltaic devices leading to the development of high power VCSELs, optical transceivers (integration of VCSELs and photo-detectors) and Monolithic Infrared (IR) Focal Plane Arrays (FPAs). The developments will be done in a phased manner as described in the following section detailing the Scope of Work.

The vendor must make sure that price information from the part-II (Price) of the two-part tender is not included in the part-I (Techno-Commercial) of the bid.

2 Eligibility Criteria

The bidder responding with an RFP shall be a competent manufacturer / developer having designed, developed and tested Gallium Arsenide technology based monolithically integrated VCSELs, photo-detectors, photovoltaic devices and MMICs. The bidder shall have established the process and have realised production quality VCSEL, photo-detectors, photovoltaic devices and MMICs. The bidder must provide supporting evidences along with the bid.

3 Scope of Work

The project will be implemented in three phases with multiple milestones for each phase having appropriate checkpoints.

In the first phase, the manufacturer / developer shall demonstrate performance of discrete devices including Enhancement and Depletion Field Effect Transistors (E-D FETs), quasi continuous wave (QCW) VCSELs (high power), VCSELs with drivers (for transceiver in communication applications), Photodetector (sensitive to 2µm) and Photovoltaic Devices. GaAs template wafers with epitaxial layers as required for the development of these devices shall be sourced by the manufacturer / developer as an optional requirement. The manufacturer / developer may submit separate price quote as an option. The manufacturer / developer shall also provide design of epitaxial layer stack for MWIR (photo-response up to 5µm) photodetector with supporting simulation results.

In the second phase of the project, the manufacturer / developer shall grow requisite epitaxial stack(s) in SCL fab. The grown epitaxial stack shall be used for demonstration of device level performance similar to those in phase 1. Using this/these epitaxial stack(s), technology demonstrator circuits shall be developed. These will include QCW VCSELs, opto-electronic transceivers, solar cell tiles, individual MWIR photodetector pixels and photodetector arrays. As part of this phase, the manufacturer / developer shall develop and provide process development kit (PDK) for SCL fab line. As a part of this phase, the

manufacturer / developer shall also provide a preliminary architectural design of the read-out integrated circuit (ROIC).

In the third phase, the manufacturer / developer shall design, develop, manufacture and transfer process technology for monolithic IRFPA.

Along with the bid, the manufacturer / developer shall provide an evaluation of SCL's existing fab line and a list of equipment / characterisation facilities required for complete installation and transfer of the offered technology. The manufacturer / developer, if required may undertake a study of SCL's fab line for this purpose. SCL reserves the right to reject a manufacturer / developer whose bid requires major capital investment for adapting the existing fab line to meet the requirements of the proposed technology.

3.1 Phase 1

The primary deliverables for the first phase of the project are a qualified baseline process for the manufacture of quasi continuous wave (QCW) VCSELs (high power), VCSELs with drivers (for transceiver targeting optical communication applications), VCSEL arrays, Quantum Dot Photodetector sensitive to 2µm wavelength and multi-junction solar cells. Also to be completed in the first phase is the design of the epitaxial layer stack for MWIR quantum dot photodetector. The detailed scope of work is given below.

3.1.1 Development details and milestones

The technology details should support the development of all the devices considered under this project and should include complete design and simulation details of all the process and design modules.

The devices should include enhancement and depletion mode FETs, VCSELs and VCSEL arrays, photovoltaic devices, as well as quantum dot photodetectors. The transfer should include all the documentation required for installation of the technology. The following activities are to be completed in the first phase of the project:

3.1.1.1 Manufacturer / developer to provide list of devices (active elements like E-D FETs, QCW VCSELs, VCSELs with drivers, photovoltaic devices and quantum dot photodetectors sensitive up to 2µm wavelength as well as passives including resistors, capacitors, inductors and varactors) offered along with complete Process Identification Document / Documents for each type of device including the complete process flow, layer stack details, equipment details (including mapping of equipment to each unit step and specifications of any speciality raw materials required), complete process details including process recipe details like growth temperature, doping conditions and Distributed Bragg Reflector (DBR) details.

3.1.1.2 Manufacturer / developer to provide the details of a technology transfer vehicle (TTV) including layout details along with appropriate documentation of the process monitoring structures required for setting up and regular monitoring of the process, test structures and any products required for fabrication and evaluation of all the devices considered in this technology transfer. The device test structures should include all the structures required to demonstrate the performance of the devices listed in point 1 above.

3.1.1.3 Based on the assessment of existing equipment set in SCL fab, manufacturer / developer to propose addition / modification in the existing equipment for meeting the requirement of the above process technology including equipment required for epitaxial layer growth.

3.1.1.4 Manufacturer / developer to provide device design (wafer and epi layer stack specifications corresponding to the different device types, device layout, TCAD simulation deck along with simulation files) along with characterisation results of devices already developed by the manufacturer / developer.

3.1.1.5 Manufacturer / developer to propose detailed training plan including photovoltaic device physics, layer stack optimization, critical parameter trade-off analysis, modelling and simulation of electrical and electro-optical performance parameters and test procedures for evaluation of device performance.

3.1.1.6 Propose plan for hands-on training to be provided to SCL engineers on the fabrication process including the equipment.

3.1.1.7 Unit step development details including recipe details, metrology requirements and success criteria for unit step establishment to be provided by the manufacturer / developer.

3.1.1.8 Manufacturer / developer to provide development details for integration of unit steps into modules along with success criteria.

3.1.1.9 Design of epitaxial layer stack for MWIR quantum dot photodetector to be fabricated at SCL in the second phase of the project, to be carried out by the manufacturer / developer. SCL team shall participate in design, modelling and simulation processes.

3.1.1.10 Packaging requirement for evaluation of individual devices is to be worked out by the manufacturer / developer.

3.1.1.11 Manufacturer / developer to provide complete test and characterisation documents including test programs for the evaluation of individual device test structures in the TTV including device parameter specifications.

3.1.1.12 Packaging and characterization of device test structures and evaluation against specs.

3.1.1.13 Delivery of Final process flow (FPF) after porting the entire process flow in SCL fab by the manufacturer / developer.

3.1.1.14 Fabrication of three batches of devices utilizing the FPF.

3.1.1.15 Packaging and performance demonstration on final devices.

3.1.1.16 Reliability test and qualification documents to be provided by the manufacturer / developer along with reliability database (if available).

3.1.1.17 The specifications of the transferred devices are provided in the Annexure to this document. They cover the following devices:

(a) Enhancement and depletion HFET devices when fabricated in the same circuit along with optical devices
(b) Stand-alone enhancement and depletion HFET parameters
(c) Stand-alone pseudo-morphic HFET parameters
(d) VCSEL specifications for communications applications
(e) VCSEL specifications – Quasi-Continuous Wave
(f) Quantum dot detectors
(g) Multi-junction Solar Cells

3.1.1.18 Phase 1 Milestones:

(a) Delivery of technology transfer documentation to SCL.
(b) Demonstration of HFETs, VCSELs, photovoltaic devices and photodetectors as per target specifications.
(c) Complete design of epitaxial layer stack for MWIR quantum dot photodetector.

3.2 Phase 2

The second phase deliverables are successful epi stack development in SCL fab, generation of process design kit (PDK) based on the final process and preliminary architectural design of Read-Out IC (ROIC) for the IR FPA. Also to be completed in the second phase is demonstration of solar cell, QCW VCSELs, optoelectronic transceiver and MWIR photo-detector.

The detailed scope of work is given below.

3.2.1 Development details and milestones

The following are the milestones for the second phase of the project along with the scope of work for this phase.

3.2.1.1 The first activity will be the development of the epitaxial stack in SCL fab. The devices developed in the first phase will be fabricated so as to meet the target specifications as demonstrated in phase 1 and to develop the PDK. This will include cryo temperature models for discrete devices, as well as the standard cell library and IPs required for the development of the circuits.

3.2.1.2 Photo-detector fabrication will be done targeting the SWIR and MWIR bands (1µm to 5µm).

3.2.1.3 Multi-junction solar cell tiles of different sizes will also be demonstrated using the optimised epi layer.

3.2.1.4 Demonstrate of QCW VCSEL for high power laser applications.

3.2.1.5 Demonstration of transceiver through monolithic integration of VCSEL, driver, photodetector receiver and readout electronics.

3.2.1.6 Phase 2 Milestones:

(a) Milestone 1: Optimization of Epi growth at SCL including top and bottom DBR.

(b) Milestone 2: Detector demonstration
Milestone 2 A: Detector Preliminary Design Review (PDR)
Milestone 2 B: Detector Critical Design Review (CDR)

(c) Milestone 3: Process finalisation and PDK development
Milestone 3A: Process, device and interconnect modelling for parasitic extraction and development of Mentor Graphics compatible deck.
Milestone 3B: PDK development including cryo temperature models for all active devices and passives across their entire operating range as well as standard cell library.
Milestone 3C: IP development including pixel level amplifier/column amplifier/row decoder/column decoder/bias generator. In addition, manufacturer / developer to develop IPs required for obtaining functionality of all circuits.
Milestone 3D: Review of architecture design for ROIC.

(d) Milestone 4: Solar cell tile demonstration (Size: 30, 60, 100mm^2)
Milestone 4A: PDR for solar cell development
Milestone 4B: Solar cell development CDR
Milestone 4C: Testing and performance evaluation using optimised Epi grown as a part of milestone 1 at SCL facility

(e) Milestone 5: Demonstration of QCW VCSELs and transceiver for wavelength finalized as a part of phase 1 development: monolithic integration of VCSEL driver (for 1GHz operation), VCSEL, receiver with compatible readout electronics.
Milestone 5A: PDR for VCSEL design
Milestone 5B: CDR for VCSEL design

Milestone 5C: Testing and performance evaluation of QCW VCSEL and transceiver fabricated in (as a part of milestone 1) SCL facility

(f) Milestone 6: Result and performance review and clearance for third phase

3.3 Phase 3

The third phase of the project will commence with design of ROIC for IR imager. Any tuning of the process to achieve the required specifications of the detector array and the on-chip integrated ROIC will also be done. As an intermediate step, the detector characteristics may be tuned to achieve target specifications by employing a proven Silicon ROIC with hybrid integration.

The design of the readout circuitry for monolithic integration with the detector array will be done in this phase.

3.3.1 Development details and milestones

The following are the milestones for the third phase of the project along with the scope of work for this phase.

(a) Milestone 1
PDR of ROIC design.
CDR1 of ROIC design.

(b) Milestone 2
Fabrication of detector array using SCL epi stack process
Bump-bonding of Si ROIC 320×256 (or any other mutually acceptable array)
Testing and performance evaluation

(c) Milestone 3
CDR2 of ROIC design and clearance for monolithic integration
Processing of readout circuitry in SCL fab
Testing and performance evaluation

(d) Milestone 4
Fabrication of monolithic IR FPA in SCL process
Testing and performance evaluation

4 Schedules

The time schedule for the project is three years. Each of the phases detailed above will be completed in one year. The second and third phases will be initiated only after all the milestones of the previous phase are completed. If required, the duration of a phase can be extended by up to three months. However, the entire project has to be completed in three years.

5 Annexures

5.1 Annexure 1: Specifications

5.1.1 Enhancement and depletion HFET devices when fabricated in the same circuit along with optical devices.

Gate Length (µm)	Type	Vg (V)	Vd (V)	Gm (typical) (mS/mm)	Ft (typical) (GHz)	Fmax (typical) (GHz)
0.25	Enhancement	1	3.3	300	95	150
0.25	Depletion	1	3.3	350	95	150
0.40	Enhancement	1	3.3	250	60	100
0.40	Depletion	1	3.3	325	60	100

5.1.2 Stand-alone enhancement and depletion HFET parameters

Gate Length (µm)	Type	Vg (V)	Vd (V)	Gm (typical) (mS/mm)	Ft (typical) (GHz)	Fmax (typical) (GHz)
0.25	Enhancement	1	3.3	525	100	160
0.25	Depletion	1	3.3	500	100	160
0.40	Enhancement	1	3.3	500	65	110
0.40	Depletion	1	3.3	475	65	110

5.1.3 Stand-alone pseudo-morphic HFET parameters

Gate Length (µm)	Type	Vg (V)	Vd (V)	Gm (typical) (mS/mm)	Ft (typical) (GHz)	Fmax (typical) (GHz)
0.25	Enhancement	1	3.3	550	100	160
0.25	Depletion	1	3.3	650	100	160
0.40	Enhancement	1	3.3	500	65	110
0.40	Depletion	1	3.3	600	65	110

5.1.4 VCSEL specifications – for communications applications

Parameter	Typical value	Remarks
Emission wavelength (nm)	850 to 980 Optional: 1550	Preferred value. Up to 940 nm is also acceptable
Emission wavelength bandwidth (nm)	2 to 3	
Peak output optical power (mW)	≥0.5	
Operating temperature (°C)	0 to 70 or better	
Temperature drift of central wavelength (nm/°C)	≤0.5	
Signal bandwidth (GHz)	≥20	
Slope efficiency (W/A)	0.1 to 0.2	
Threshold current (mA)	1 (typical)	
Capacitance (fF)	≤300	
Relative Intensity Noise (dB/Hz)	≤130	
Laser mode	Single or multi mode	Single mode is preferred
Beam profile	Gaussian	
Operating voltage (V)	2.5	

5.1.5 VCSEL specifications – Quasi-Continuous Wave

Parameter	Typical value	Remarks
Emission wavelength (nm)	850 to 980 Optional: 1550	Preferred value. Up to 940 nm is also acceptable
Emitter type	VCSEL (array)	
Emission mode	Single Mode, circular beam profile preferred	Vertical emission preferred. However, the manufacturer / developer may propose an alternative option with edge emitter, meeting the requirements. The manufacturer / developer shall bring out specific advantages, if any in the proposed technology. In case such an alternative option is proposed and found to be advantageous, it would be considered.
Output type	QCW, Duty cycle-0.1% or more	

Parameter	Typical value	Remarks
	(30Hz)	
Emission wavelength bandwidth (FWHM, nm)	2 to 3	
Output optical power (W)	≥10	
Operating temperature (°C)	0 to 70 or better	
Temperature drift of central wavelength (nm/°C)	≤0.1	
Power conversion Efficiency (with the operating temperature)	≥30%	
Emission area	5mm x 5mm	

5.1.6 Quantum dot detectors

Parameter	Typical Value	Remarks
Wavelength band (μm)	1 to 5	First phase of project: 1 to 2 Second phase: 1 to 5
Specific detectivity (cm $Hz^{1/2}$ / W)	≥1e10	
Quantum efficiency	≥0.1	
Dark current for pixel of 30μm^2 (pA)	≤100	
NETD (mK)	≤30	

5.1.7 Multi-junction Solar Cells

The multi junction solar cells to be demonstrated shall belong to the space qualified InGaP / GaAs family and its variants. The minimum efficiency will be 28% at one sun illumination (AM0) at 28°C.

Basic parameters like open circuit voltage and short circuit current, as well as the maximum power point current and voltage shall be demonstrated.

5.1.8 IRFPA Specifications

The detector array for demonstration of the technology will be a 320×256 element array with 30μm square pixels. The broad specifications will be as follows:

Signal capacity: ≥$10x10^6$ electrons
Quantum efficiency: ≥10%
Dark rate: ≤100pA/pixel at 100K
NETD: ≤50mK
Noise floor: ≤1000electrons
Operating temperature: ≥100K